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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | | ATTORNEY DOCKET NO. |
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| 09/184,388 | 09/30/98 | CHIN | H | CISCP054 |

022434
BEYER WEAVER & THOMAS LLP
P.O. BOX 778
BERKELEY CA 94704-0778

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| EXAMINER | |
|---|---|
| PRIETO, B | |
| **ART UNIT** | **PAPER NUMBER** |
| 2152 | 4 |

**DATE MAILED:** 01/18/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

# Office Action Summary

| Application No. | Applicant(s) |
|---|---|
| 09/164,388 | CHIN |
| **Examiner** | **Group Art Unit** |
| Beatriz Prieto | 2152 |

☒ Responsive to communication(s) filed on *IDS filed 02/22/99*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

**Disposition of Claim**

☒ Claim(s) *1-44* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-44* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

**Application Papers**

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

*--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---*

## *Detailed Action*

### *Drawings*

1. Drawings have been objected to by the Draftsperson under 37 CFR 1.84 or 1.152, correction noted on PTO-948 is required.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1-42** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Calvignac et. al. (Calvignac)** U.S. Patent No. **5,333,269** in view of **Kurita et. al. (Kurita)** U.S. Patent No. **5,920,568.**

Regarding claims 1, 4, 10, 19 and 20, Calvignac teaches substantial features of the invention as claimed; Calvignac teaches method/apparatus for providing an inbound/outbound controller for an interconnecting/routing device, said device having an inbound adapter and an outbound adapter, a memory, and a CPU (abstract, Figs. 1, 8, 17)), the inbound controller being adapted for receiving an inbound packet at the inbound receiving adapter means (col 1/lines 29-37, col 1/lines 60-col 2/line 6 and storing inbound packet at inbound queue), the outbound controller being adapted for forwarding packets at the corresponding outbound transmitting adapter means (col 2/line 10-35, col 3/lines 4-col 4/line 41, col 17/lines 49-52 and storing forward packet at outbound queue), the method comprising: means/apparatus for determining when one of the plurality of inbound queues is ready to be moved to a corresponding outbound queue (col 12/lines 3-col 13/line 28), means/apparatus for receiving an instruction signal to handle an inbound queue, the inbound queue storing a plurality of packets (col 9/lines 7-19, col 12/lines 3-col 13/line 28); and means/apparatus for repeating the steps of receiving, providing, and storing until an instruction signal is asserted and received, initiating the said transfer step (Fig. 19A-B, 20-21).

However Calvignac does not explicitly teach where means/apparatus for classifying the inbound packet in a selected one of the plurality of inbound queues according to packet sorting

criteria; transferring one of plurality of inbound queue to one of the plurality of outbound queues corresponding to the packet sorting criteria;

Kurita teaches a system/method related to packet forwarding through manipulating multiple queues of packet, disclosing a method/apparatus for providing an inbound/outbound controller for a router (Fig. 1 (11, 10), Fig. 6, (10), Fig. 7, (31, 38), Fig. 13 (50)), the router having an inbound port (Fig. 7 (31)) and an outbound port (Fig. 7 (38)), a memory, and a CPU (Fig. 7, (33-34)), the inbound controller being adapted for receiving an inbound packet at the inbound port, the outbound controller being adapted for forwarding packets (Fig. 2) at the outbound port, the method comprising: means/apparatus for classifying the inbound packet in a selected one of the plurality of inbound queues according to packet sorting criteria (Kurita: Fig. 1, (11), Fig. 7, (33), col 1/lines 26-39, col 5/lines 44-56); means/apparatus for providing a plurality of inbound queues for the inbound port (Kurita: col 1/lines 35-62, col 5/lines 44-56); and receiving an inbound packet at the inbound port; sorting means coupled to classifier means being capable of storing the inbound packet in the selected one of the plurality of inbound queues a plurality of inbound queues (Fig. 1, (12), Fig. 7, (32)); and transferring the inbound queue to the outbound queue, the inbound queue corresponding to the sorting criteria to the outbound queue (Kurita: col 8/lines 62-67, col 9/line 1-col 10/line 53);

It would have been obvious to one ordinary skilled in the art at the time the invention was made to modify Calvignac's system with means/apparatus for classifying the inbound packet in a selected one of the plurality of inbound queues according to packet sorting criteria; transferring one of plurality of inbound queue to one of the plurality of outbound queues corresponding to the packet sorting criteria, as taught by Kurita, enabling means for repeating the steps of receiving, providing, classifying, and storing until an instruction signal is asserted and received, initiating the said transfer step. Motivation would to provide a scheme suitable for use with routers and contrived to read data elements from a plurality of queues, scheme characterized in that the maximum value of time needed till the data elements are taken from within the queue does not depend on the number of data elements in other queues, where each queue treated impartially and the packets can be communicated without any decline in the throughput property.

Regarding claim 2, the combined teachings of Calvignac and Kurita as discussed above, the method further including: asserting an interrupt when it is determined that one of the plurality of inbound queues is ready to be moved to an outbound queue (Calvignac: col 12/lines 22-37, col 9/lines 7-19, col 12/lines 3-col 13/line 28).

Regarding claim 3, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein classifying the inbound packet includes: selecting inbound packet sorting criteria (Kurita: col 8/lines 62-67); obtaining packet sorting data for the inbound packet, the packet sorting data being associated with the packet sorting criteria; and sorting the inbound packet into one of the plurality of inbound queues according to the packet sorting data (Kurita: col 1/lines 236-62, col 5/lines 44-56, col 8/lines 62-67, col 9/line 1-col 10/line 53);

Regarding claim 5, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein storing the inbound packet includes: means/apparatus for obtaining an available packet buffer from a free pool of available packet buffers; placing the inbound packet in the packet buffer; and storing the packet buffer in the inbound queue (Calvignac: col 2/lines 1-19, 29-35, col 5/lines 20-22).

Regarding claim 6, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein determining when one of the plurality of inbound queues is ready to be moved to an outbound queue includes: determining whether a number of packets in one of the plurality of inbound queues exceeds a maximum number of packets (Calvignac: col 6/lines 22-25, col 7/lines 52-65, Fig. 11B, 13A).

Regarding claim 7, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein determining when one of the plurality of inbound queues is ready to be moved to an outbound queue includes: determining whether a number of bytes in one of the plurality of inbound queues exceeds a maximum number of bytes (Calvignac: Fig. 10A).

Regarding claim 8, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein determining when one of the plurality of inbound queues is ready to be moved to an outbound queue further includes: determining whether a free pool of available memory has been depleted (Calvignac: Fig. 16, (271), col 8/lines 14-41, determination means: col 15/lines 41-col 16/line 54).

Regarding claim 9, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein determining when one of the plurality of inbound queues is ready to be moved to an outbound queue further includes: determining whether a maximum time limit has been exceeded (Calvignac: col 16/lines 30-36).

Regarding claim 11, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein receiving the instruction signal includes: receiving a notification from the controlling processor to handle the inbound queue (Calvignac: col 9/lines 7-19, col 12/lines 3-col 13/line 28).

Regarding claim 12, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus further including: transmitting packets stored in the outbound queue (Calvignac: Fig. 23, functions performed by logic 506 and 508 for transmitting data packet bursts to the destination).

Regarding claim 13, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein transmitting packets includes: selectively discarding packets stored in the outbound queue (Calvignac: col 7/lines 4-6, releasing means, col 14/lines 33-col 15/line 4).

Regarding claim 14, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein transmitting packets stored in the outbound queue further includes: obtaining a next one of the plurality of inbound queues stored in the outbound queue; transmitting selected packets stored in the next one of the plurality of inbound queues; and releasing memory associated with the next one of the plurality of inbound queues (Calvignac: col 7/lines 4-6, releasing means, col 14/lines 33-col 15/line 4, Fig. 10A-B, (121)).

Regarding claim 15, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein releasing the memory includes: storing the released memory in a free pool of available packet buffers (Calvignac: col 27/lines 36-61).

Regarding claim 16, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein releasing the memory includes: forming a new inbound queue to be used by an inbound controller (Calvignac: col 14/lines 5-19).

Regarding claim 17, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein releasing the memory includes: forming a queue to be used by the outbound controller during bi-directional operation (Calvignac: Fig. 26).

Regarding claim 18, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein transferring the inbound queue to the outbound queue further includes: ascertaining a priority of the inbound queue based on a predetermined criteria; and transferring the inbound queue to the outbound queue according to the said priority of the inbound queue (Kurita: col 8/lines 62-67, col 9/line 1-col 10/line 53).

Regarding claim 21, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus further including: a module adapted for providing the determined one of the plurality of inbound queues (Calvignac: col 1/lines 26-39, col 5/lines 44-56, col 12/lines 22-37, col 9/lines 7-19, col 12/lines 3-col 13/line 28).

Regarding claim 22, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus further including: a module adapted for asserting an interrupt when it is determined that one of the plurality of inbound queues is ready to be moved by the CPU to the outbound queue (Calvignac: col 12/lines 22-37, col 9/lines 7-19, col 12/lines 3-col 13/line 28).

Regarding claim 23-27, this claim comprises the apparatus associated with the method disclosed on claim 5-9, respectively, same rationale is applicable.

Regarding claim 28, this claim comprises the apparatus associated with the method disclosed on claims (1, 4, 10, and 19-20) and 10, same rationale is applicable.

Regarding claim 29-36, this claim comprises the apparatus associated with the method disclosed on claims 11-18, respectively, same rationale is applicable.

Regarding claim 37, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein a router having a plurality of inbound ports and a plurality of outbound, ports, a memory, and a CPU, comprising: an inbound controller coupled to one of the plurality of inbound ports, the inbound controller being adapted for receiving an inbound packet and storing inbound packet at inbound queue; (Calvignac abstract, Figs. 1, 8, 17, col 1/lines 29-37, col 1/lines 60-col 2/line 6 and storing inbound packet at inbound queue); wherein the memory has stored therein: a plurality of inbound queues for the one of the plurality of inbound ports; and a plurality of outbound queues, each one of the plurality of outbound queues corresponding to one of the plurality of outbound ports and being capable of storing a plurality of inbound queues (Calvignac: col 2/line 10-35, col 3/lines 4-col 4/line 41, col 17/lines 49-52, col 12/lines 3-col 13/line 28); a classifier coupled to the inbound controller, the classifier being adapted for classifying the inbound packet in a selected one of the plurality of inbound queues according to packet sorting criteria, the selected one of the plurality of inbound queues being associated with one of the plurality of

outbound queues; wherein the inbound controller is adapted for storing the inbound packet in the selected one of the plurality of inbound queues (Kurita: Fig. 1-2, 6, 7, 13), col 1/lines 26-62, col 5/lines 44-56, col 8/lines 62-67, col 9/line 1-col 10/line 53);

Regarding claim 38, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus further including: an outbound controller coupled to the inbound controller; wherein the inbound controller selects one of the plurality of inbound queues to be transferred to the outbound controller; wherein the outbound controller is adapted for storing the selected one of the plurality of inbound queues in one of the plurality of outbound queues associated with the packet sorting criteria and transmitting packets stored in the one of the plurality of outbound queues (Calvignac abstract, Figs. 1, 8, 17, col 1/lines 29-37, col 1/lines 60-col 2/line 6, col 2/line 10-35, col 3/lines 4-col 4/line 41, col 17/lines 49-52, col 12/lines 3-col 13/line 28, Kurita: Fig. 1-2, 6, 7, 13), col 1/lines 26-62, col 5/lines 44-56, col 8/lines 62-67, col 9/line 1-col 10/line 53);

Regarding claim 39, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein the inbound controller further includes: a memory obtaining module coupled to the classifier, the memory obtaining module being adapted for obtaining memory for an inbound packet to permit the inbound packet to be stored in the selected one of the plurality of inbound queues in which the inbound packet is classified (Kurita: col 8/lines 62-67, col 1/lines 236-62, col 5/lines 44-56, col 8/lines 62-67, col 9/line 1-col 10/line 53) .

Regarding claim 38, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein the outbound controller further includes: a memory releasing module adapted for releasing selected packet buffers associated with packets stored in the one of the plurality of outbound queues (Calvignac: Fig. 23, functions performed by logic 506 and 508 for transmitting data packet bursts to the destination).

Regarding claim 39, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein transmitting packets includes: selectively discarding packets stored in the outbound queue (Calvignac: col 7/lines 4-6, releasing means, col 14/lines 33-col 15/line 4).

Regarding claim 40, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein transmitting packets stored in the outbound queue further includes: obtaining a next one of the plurality of inbound queues stored in the outbound queue; transmitting selected packets stored in the next one of the plurality of inbound queues; and releasing memory associated with the next one of the plurality of inbound queues (Calvignac: col 7/lines 4-6, releasing means, col 14/lines 33-col 15/line 4, Fig. 10A-B, (121)).

Regarding claim 41, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein the memory further includes a free pool of available packet buffers and the memory releasing module is adapted for releasing the selected packet buffers into the free pool (Kurita: col 8/lines 62-6, col 1/lines 236-62, col 5/lines 44-56, col 8/lines 62-67, col 9/line 1-col 10/line 53).

Regarding claim 42, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus wherein the outbound controller further includes: a memory releasing module

adapted for providing a new inbound queue to the inbound controller to replace the selected one of the plurality of inbound queues Calvignac: col 14/lines 5-19).

4. Claims **43-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Calvignac et. al. (Calvignac)** U.S. Patent No. **5,333,269** in view of **Kurita et. al. (Kurita)** U.S. Patent No. **5,920,568** in further view of **Finkelstein et. al. (Finkelstein)** U.S. Patent No. **5,319,712**.

Regarding claim 43, the combined teachings of Calvignac and Kurita as discussed above, the method/apparatus comprising: an inbound controller adapted for receiving an inbound packet; a classifier coupled to the inbound controller and adapted for classifying and storing the inbound packet in an inbound queue; an outbound controller adapted for receiving the inbound queue * (Calvignac: abstract, Figs. 1, 8, 17, Fig. 19A-B, 20-21, col 1/lines 29-37, col 1/lines 60-col 2/line 6, col 2/line 10-35, col 3/lines 4-col 4/line 41, col 17/lines 49-52, col 12/lines 3-col 13/line 28, col 9/lines 7-19, col 12/lines 3-col 13/line 28: Kurita: Fig. 1, 2, 6, 7,. 13 col 1/lines 26-39, col 5/lines 44-56: col 1/lines 35-62, col 5/lines 44-56, col 8/lines 62-67, col 9/line 1-col 10/line 53);

however the combined teachings of Calvignac nor Kurita explicitly teach encryption means wherein an encryption box coupled to the outbound controller, the encryption box being adapted for encrypting the inbound queue to provide an encrypted inbound queue to the outbound controller for transmission.

Finkelstein teaches encryption means wherein an encryption box coupled to the outbound controlling means, the encryption box being adapted for encrypting the inbound buffer to provide an encrypted inbound buffer to the outbound controlling means for transmission (Finkelstein: col 6/line 52-col 7/line 35).

It would have been obvious to one ordinary skilled in the art at the time the invention was made to modify existing system with encryption means wherein an encryption box coupled to the outbound controller, the encryption box being adapted for encrypting the inbound queue to provide an encrypted inbound queue to the outbound controller for transmission, as taught by Finkelstein, motivation would be to implement a robust encryption scheme that may be implemented on interconnecting/switching devices operating either on the 2 or 3 protocol layer of the OSI model for user either the communication unit or base site communication unit of a cellular communication system, where the direction of transmission between the transmitting portion and the receiving portion may be either uplink (i.e., subscriber unit to base site unit) or downlink (i.e., base site unit to user device).

Regarding claim 44, the combined teachings of Calvignac and Kurita as discussed above, wherein wherein the outbound controller includes an outbound classifier adapted for classifying the encrypted inbound queue in an outbound queue, the outbound controller adapted for transmitting data stored in the outbound queue (Kurita inbound/outbound controller for a router (Fig. 1 (11, 10), Fig. 6, (10), Fig. 7, (31, 38), Fig. 13 (50)), the router having an inbound port (Fig. 7 (31)) and an outbound port (Fig. 7 (38)), the inbound controller being adapted for receiving an inbound packet at the inbound port, the outbound controller being adapted for forwarding, means/apparatus for classifying the inbound packet in a selected one of the plurality of inbound queues according to packet sorting criteria (Kurita: Fig. 1, (11), Fig. 7, (33), col 1/lines 26-39, col 5/lines 44-56); means/apparatus for providing a plurality of inbound queues for the inbound port (Kurita: col

1/lines 35-62, col 5/lines 44-56, col 8/lines 62-67, col 9/line 1-col 10/line 53, Finkelstein: col 6/line 52-col 7/line 35).

***Citation of Pertinent Art:***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure; Copies of documents cited will be provided as set forth in MPEP § 707.05(a):

| | | |
|---|---|---|
| Ref A: U.S. Patent No. 6,157,623, | Kerstein, | 12/05/00 |
| Ref B: U.S. Patent No. 6,134,619 | Futral et. al. | 10/17/00 |
| Ref C: U.S. Patent No. 6,101,170 | Doherty et. al. | 08/08/00 |
| Ref E: U.S. Patent No. 5,925,099 | Futral et. al. | 07/20/99 |
| Ref F: U.S. Patent No. 5,907,717 | Ellis | 05/25/99 |

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Beatriz Prieto** whose telephone number **is (703) 305-0750**. The Examiner can normally be reached on Monday-Friday from 6:30 to 4:00 p.m. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's Supervisor, **Mark H. Rinehart** can be reached on **(703) 305-4815**. The fax phone number for the organization where this application or proceeding is assigned is **(703) 308-6606**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is **(703) 305-3800/4700.**

B. Prieto
Patent Examiner
January 8, 2001

LE HIEN LUU
PRIMARY EXAMINER